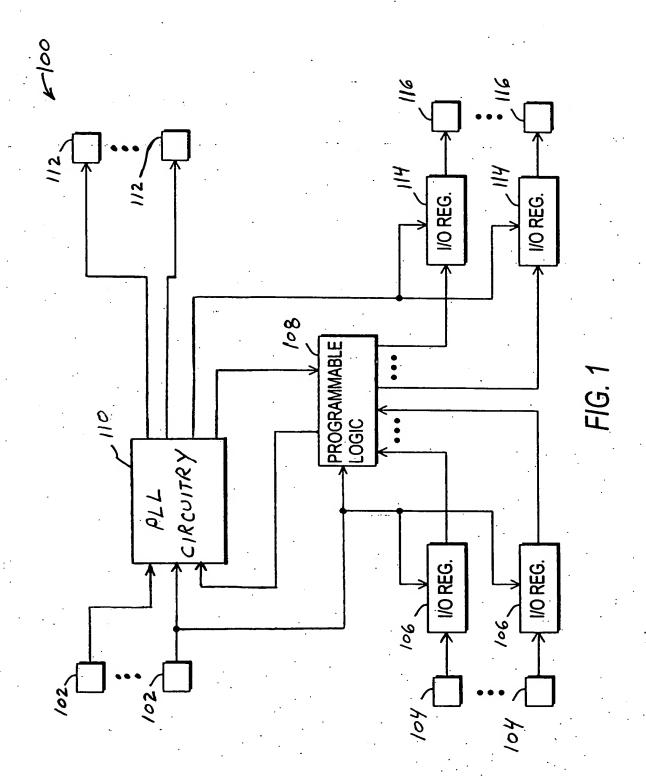
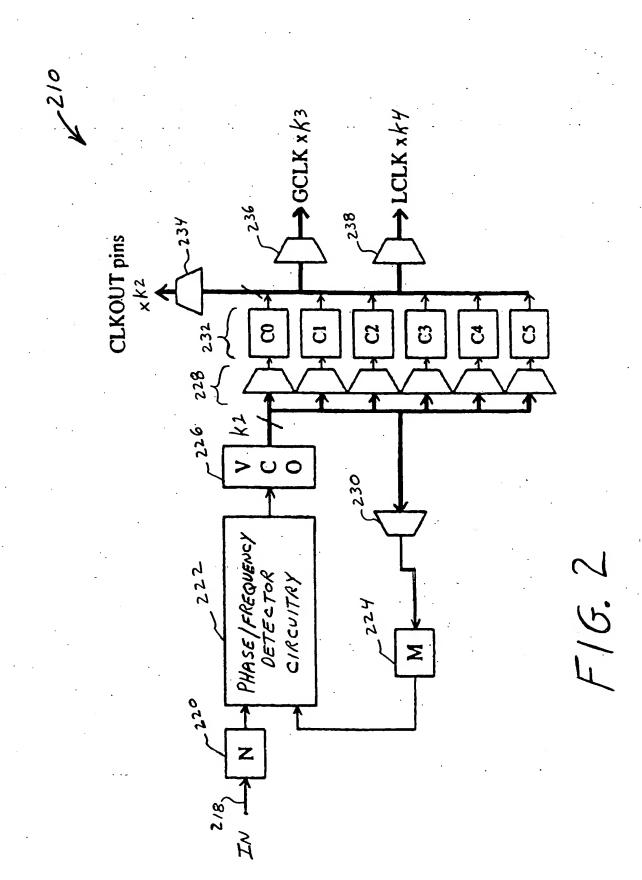
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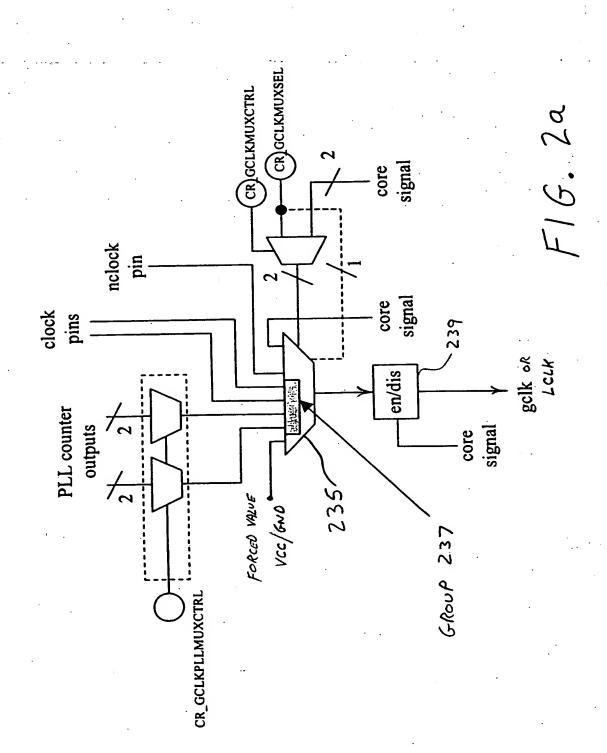


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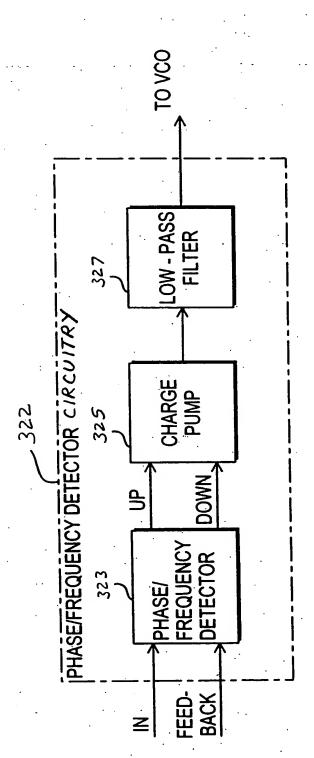
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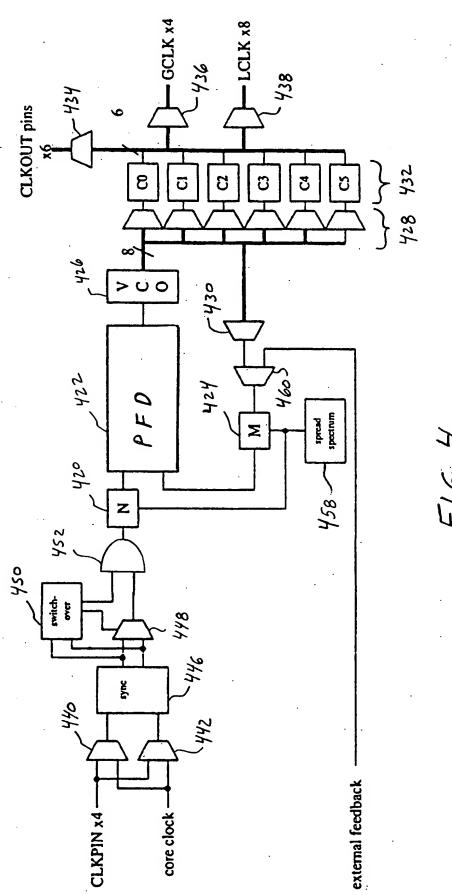
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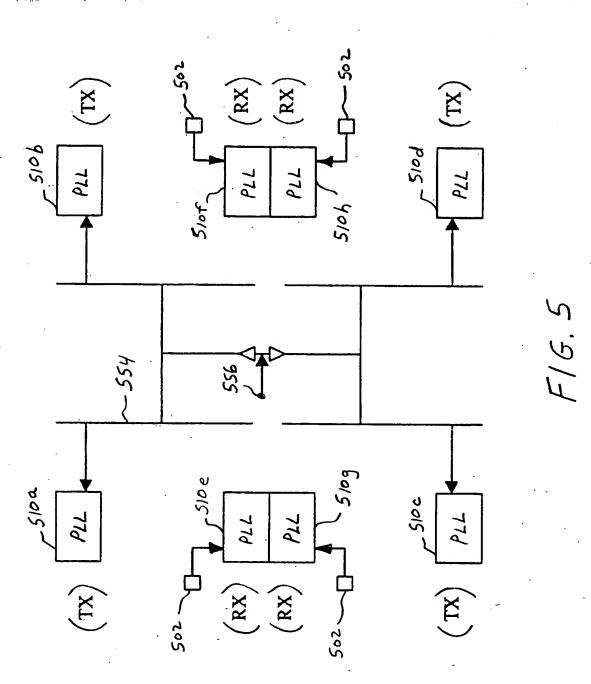


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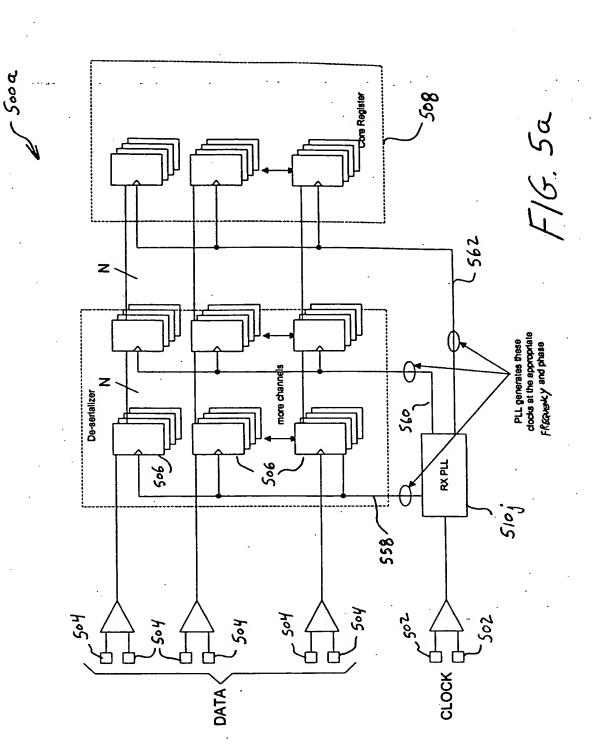


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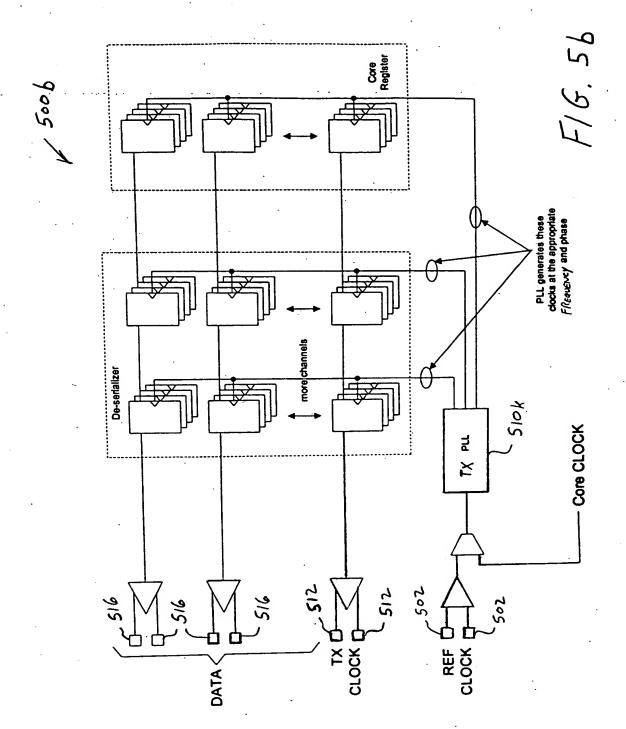




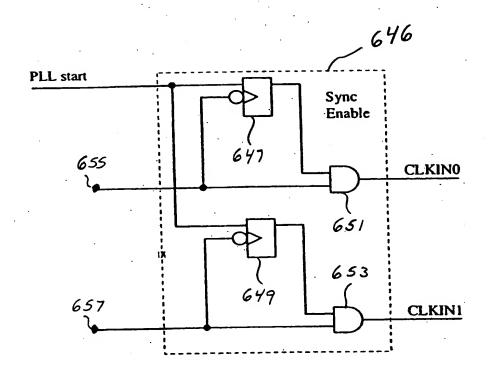
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F16.6

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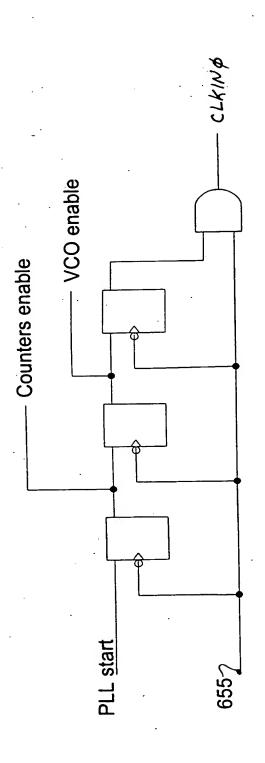
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CI CZ **C3** - C4 CS CLKPIN12 PLL CLKPIN13 CLKPIN14 CLKPIN15 710 nCLKPIN12 nCLKPIN13 DLLCLK. nCLKPIN14 nCLKPIN15 **GCKDRV0** core signal **GCKDRVI** input to clock GCKDRV2 petwork **GCKDRV3** LCKDRV0 LCKDRV 1 LCKDRV 2 core signal LCKDRV 3 input to clock LCKDRV4 network LCKDRV5 710 LCKDRV6 LCKDRV7 ∞ CI CZ PLL GCK12 &CK13 GCK14 GCK15 LCK24 LCK25 LCK26 LCK27 LCK28 LCK29 LCK30 LCK31

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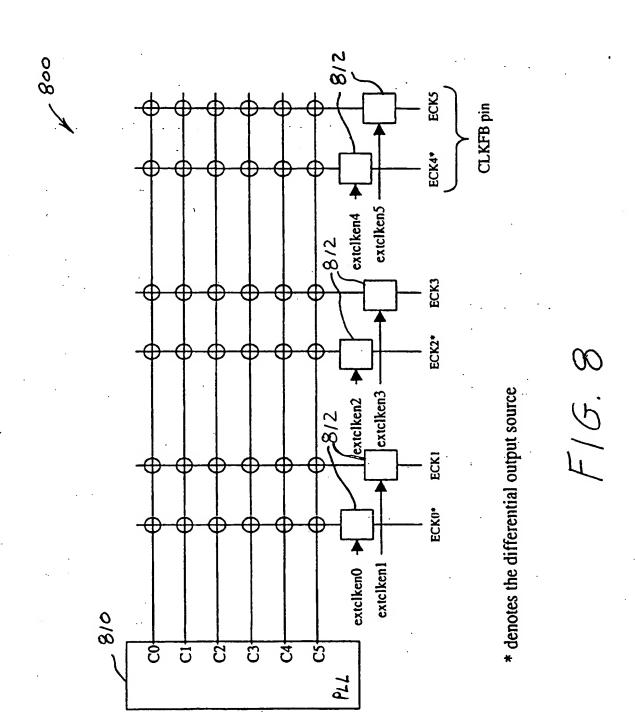
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F16.7

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928 932 VCO/ test clk C0 VCO/ test clk VCO/ test clk VCO/ test clk VCO/ test clkC4 VCO/ test clk **C**5

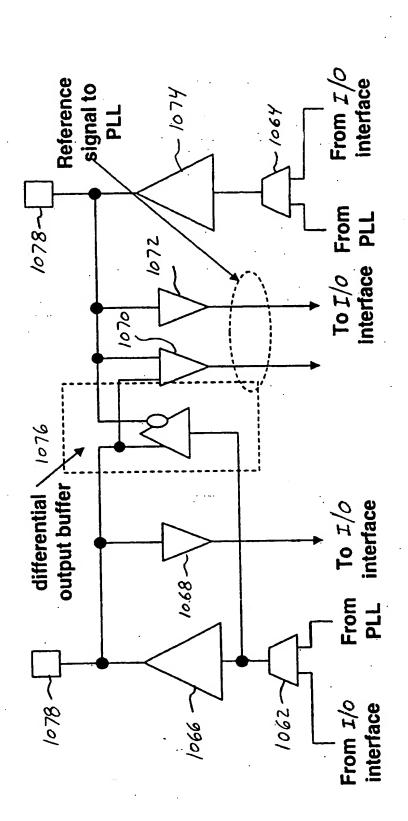
F16.9

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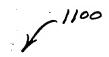
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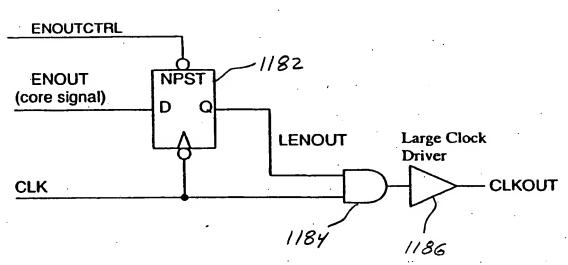


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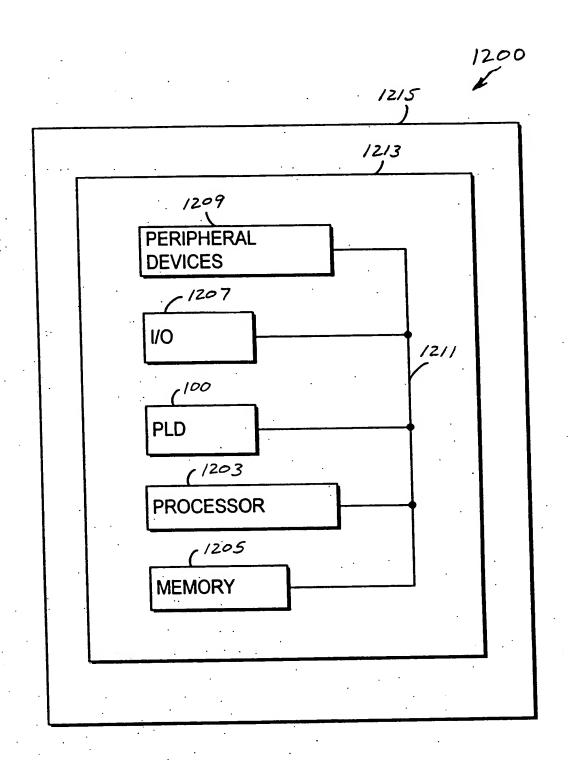


FIG. 12